800G OSFP DR8 Transceiver, SMF 8×100G PAM4 1310nm, 500M

Features

- 8x53.125Gbps electrical interface
- 8x106.25Gbps optics architecture
- Up to 500m transmission on single mode fiber (SMF) with FEC
- Hot Pluggable OSFP form factor
- 8 channels 1311nm EML Laser
- 8 channels PIN photo detector
- Commercial operating case temperature range: 0~ 70ºC
- RoHS Compliant(lead free)
- Power dissipation < 16.5 W
- TDECQ<3.4dB
- MPO-16/APC optical connectors
- OSFP MSA5.0 and CMIS5.1 compliant
- IEEE802.3ck and IEEE 802.3df compliant

Application

- 800GBASE Ethernet
- Data center networks
- InfiniBand NDR applications

Ordering Information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (℃)	Reach (M)	DDM
ELOM800G-OSFP-DR8-S	OSFP	800G	1311 EML	-2.9~4	Pin	＜-5.3	0~70	500	Y

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Ambient Temperature	T_{STG}	-40	85	℃
Operating Humidity	H_O	5	95	%
Power Supply Voltage	Vcc	-0.5	3.6	V
Signal Input Voltage		Vcc-0.3	Vcc +0.5	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		70	℃
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Data Rate, each Lane（PAM4）			106.25		Gbps
Power Consumption	P DISS			16.5	W
Pre-FEC Bit Error Ratio				2.4x10 -4	
Fiber Length 09/125μm core SMF		-		500	M

Optical Characteristics

Optical transmitter Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Launched Power (avg.) Per Lane	Pavg	-2.9		4	dBm	
Wavelength Range	λ	1304.5	1311	1317.5	nm	
Outer Optical Modulation Amplitude for TDECQ < 1.4dB for 1.4dB ≤ TDECQ ≤ 3.4dB		-0.8 -2.2+TDECQ		4.2	dBm	
Launch Power in OMA outer minus TDECQ, each Lane				2	dB	
Extinction Ratio	ER	3.5			dB	
Average Launch Power per Lane @ TX Off State	POff			-15	dBm	
Transmitter Eye Closure for PAM4(TECQ), each Lane				3.4	dB	
Transmitter and dispersion Eye Closure for PAM4(TDECQ), each Lane				3.4	dB	
Relative Intensity Noise (OMA)				-132	dB/Hz	
Side-Mode Suppression Ration (SMSR)		30			dB	
Optical Return Loss Tolerance				15.6	dB	

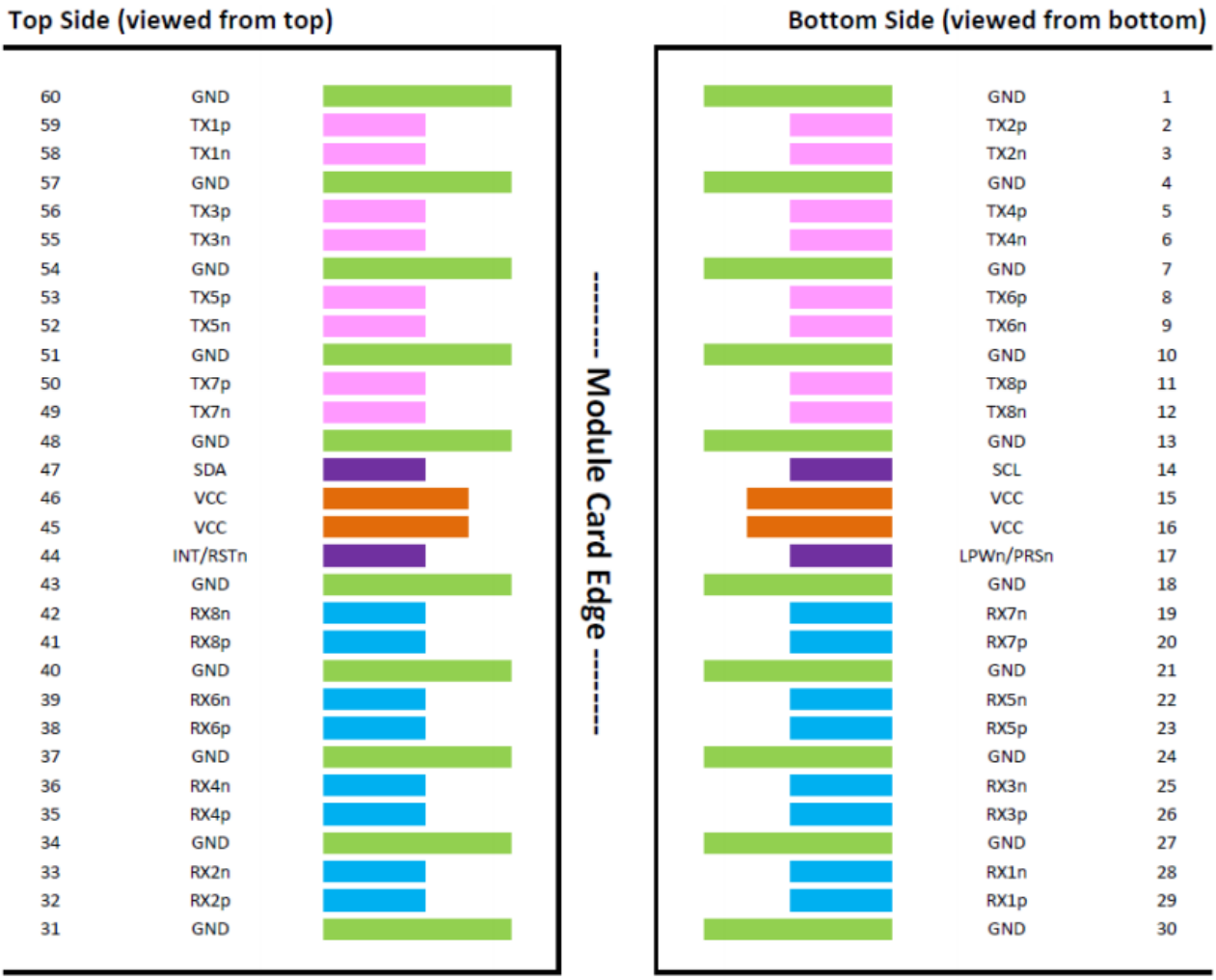
Transmitter Reflectance				-26	dB	
Transmitter over/under-shoot				25	%	
Transmitter peak-to-peak power				5.7	dBm	
Transmitter transition time				17	Ps	

Optical receiver Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver Wavelength Range	λ	1304.5	1311	1317.5	nm	
Average Receiver Power Per Lane		-5.9		4	dBm	
RX Sensitivity (OMAouter) for TECQ < 1.4dB for 1.4dB ≤ TECQ ≤ 3.4dB	Sen			 -3.9 -5.3+TECQ	dBm	1
Stressed RX Sensitivity (OMA_{outer})				-1.9	dBm	
Stressed Receiver Sensitivity in OMAouter				-4.2	dBm	1
Receiver Reflectance	Rr			-26	dB	
LOS Assert		-10			dBm	
LOS De-Assert – OMA				-8	dBm	
LOS Hysteresis		0.5			dB	

Note:

1 . Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Pin Definition



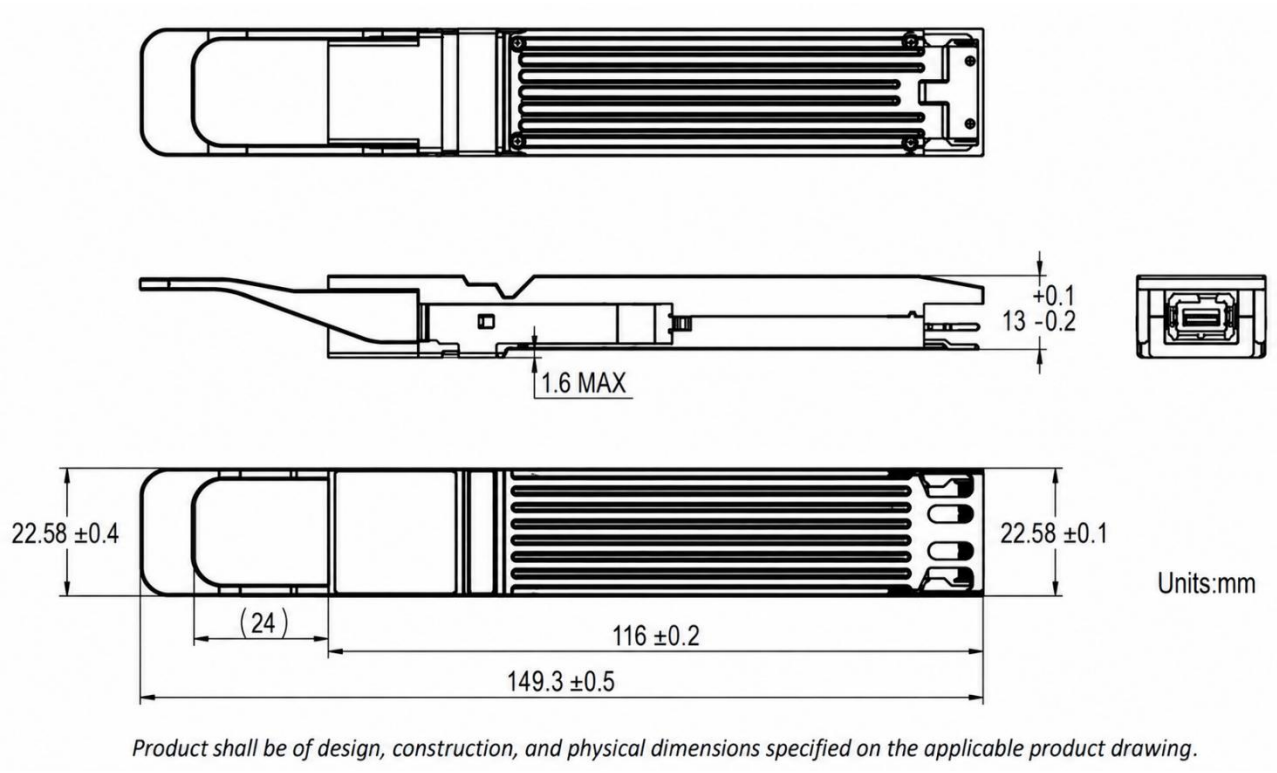
OSFP MSA-compliant 60-pin connector

The INT/RSTn signal operates in three voltage zones to indicate the Reset state for the module and Interrupt state for the host. The host uses a 2.5 V reference to determine H_INT, while the module uses a 1.25 V reference to determine M_RSTn.

ELLAX – OSFP800 DR8 Pin Definition
Compliant with OSFP MSA Rev. 5.22 Connector Pin List

Pin	Signal	Description	Logic	Direction	Pin Type	Remarks
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Package Outline



Product shall be of design, construction, and physical dimensions specified on the applicable product drawing.

Regulatory Compliance

Feature	Test	Method
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>1000V for SFI pins, >2000Vfor other pins.)
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2	Class 2(>4.0kV)
Electromagnetic Interference (EMI)	CISPR22 ITE Class B FCC Class B CENELEC EN55022 VCCI Class 1	Comply with standard
Immunity	IEC61000-4-3	Comply with standard
Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Compatible with Class I laser Product